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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,667	10/01/2003	Soo-Guy Rho	9649-479CTDVCT2	8980

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EXAMINER	
CHOWDHURY, TARIFUR RASHID	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 10/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,667	RHO ET AL.	
	Examiner	Art Unit	
	Tarifur R Chowdhury	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *46-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *53-56* is/are allowed.

6)☒ Claim(s) *46-52* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 46-49, 51 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al., (Kim), USPAT 6,100,9540 in view of Zhang et al., (Zhang), USPAT 6,222,595.

3. Kim discloses (fifth preferred embodiment; col. 18, line 40- col. 19, line 40) and shows in Fig. 14C, a thin film transistor substrate for a liquid crystal display comprising:

- a first insulating substrate (111);
- a gate pattern including a gate and a gate line electrode (113) on the transparent insulating substrate (111);

- a gate insulating layer (157) on the gate electrode (113) and comprising organic insulating material;
- a patterned silicon nitride layer (177);
- a semiconductor layer (119) disposed on the gate insulating layer (157);
- a data pattern that comprises a source electrode (123) and a drain electrode (127), which are disposed on the semiconductor layer and a data line (125) that is connected to the drain electrode;
- a protection film (159) (applicant's passivation layer) that comprises organic insulating material (col. 18, line 67) and has a contact hole that exposes the drain electrode (127); and
- a pixel electrode (131) connected to the drain electrode (127) through the first contact hole.

Even though Kim does not explicitly show the second insulating substrate, inherently a liquid crystal display includes a second substrate facing the first substrate to sandwich the liquid crystal materials in between.

Kim differs from the claimed invention because he does not explicitly disclose the limitation such as a spacer is disposed at a region where a black matrix overlaps the gate line or the data line.

Zhang shows a conventional liquid crystal display wherein a spacer (112) is disposed at a region wherein a black matrix (108) overlaps the gate line (104) and the data line (106) (Fig. 1A).

Zhang is evidence that ordinary workers in the art would find a reason, suggestion or motivation to dispose a spacer at a region wherein a black matrix overlaps the gate line or the data line.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to modify the display device of Kim by first forming a black matrix such that it overlaps either the gate line or the data line to prevent any light leakage between the signal lines and the pixel electrode and then form spacers at the region wherein the black matrix overlaps the gate line or the data line to determine the cell gap of the liquid crystal display.

Accordingly, claim 46 would have been obvious.

As to claim 47, Kim also discloses that the organic material used to form the passivation layer has superior properties of dielectric constant of 2.3 to 2.4 (col. 14, lines 10-12).

As to claim 48, Kim shows in Fig. 14C that the passivation layer (159) has a flat surface.

As to claim 49, Kim also shows in Fig. 14C that the pixel electrode (131) at least overlaps the data pattern.

As to claim 51, Kim discloses (col. 19, line 4-11) and shows in Fig. 14D that a etch stopper (135) is formed between the semiconductor layer (119) and the passivation layer (159).

As to claim 52, forming black matrix using photolithography is common and known in the art and thus would have been obvious to avail a proven technique.

4. Claims 46-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art (AAPA).

5. The AAPA described in pages 1-3 and shown in Fig.1 of the present application discloses a thin film transistor substrate for a liquid crystal display comprising:

- a transparent insulating substrate (1);
- a gate pattern including a gate electrode (2) and a gate line (not shown) on the transparent insulating substrate (1);
- a gate insulating layer (4) on the gate electrode (2);
- a semiconductor layer (5) on the gate insulating layer (4);
- a source electrode (8) and a drain electrode (9), which are separated from each other on the semiconductor layer (5);
- a data line electrically connected to the source electrode (not shown);
- a passivation layer (10) having a first contact hole exposing the drain electrode (9); and
- a pixel electrode (12) connected to the drain electrode (9) through the first contact hole;

The AAPA described in the instant application also discloses that a second insulating substrate is placed opposite to the first insulating substrate and spacers are placed between the first insulating substrate and the second insulating substrate (page 2, line 22 – page 3, line 1).

The AAPA described in the instant application further discloses (page 2, line 17, page 3, line 10) and shows in Fig. 1 that a black matrix that overlaps the gate line or the

data line is disposed in a groove of the passivation layer and spacers are disposed between the substrates to maintain a uniform cell gap. Further, since spacers are provided to keep an uniform gap between the substrates, it would have at least been obvious to one of ordinary skill in the art that the spacers are provided on top of the black matrix since the black matrix (11) is one of the top most layer of the insulating substrate (1).

The AAPA described in the instant application differs from the claimed invention because it does not explicitly disclose the limitation such as the passivation layer with flat surface comprising organic insulating material with low dielectric constant (such as 2.4-3.7). However, it is common and known in the art to use an organic material with low dielectric constant for forming a passivation layer with flat surface so that the pixel electrode can overlap the data pattern and thus an improved aperture ratio can be obtained. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to employ a passivation layer that has a flat surface and is made of an organic material having low dielectric constant so that the pixel electrode can overlap the data pattern and thus improved aperture ratio is obtained.

Accordingly, claims 46-50 would have been obvious.

As to claim 51, the AAPA described in the present application also shows in Figure 1 that an etch stopper (6) is formed between the passivation layer (10) and the semiconductor layer.

As to claim 52, forming black matrix using photolithography is common and known in the art and thus would have been obvious to avail a proven technique.

Allowable Subject Matter

6. Claims 53-56 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

As to claim 53, the prior arts of record do not anticipate or render obvious to one skilled in the art a thin film transistor substrate for a liquid crystal display comprising various elements as claimed, more specifically a metal pattern disposed over the storage capacitor electrode and is disposed on the same layer with the data line, a passivation layer comprising an organic material and is disposed on the semiconductor layer and the data line, and has a contact hole exposing the metal pattern, a pixel electrode connected to the metal pattern through the contact hole and wherein the passivation layer contacts a portion of the semiconductor layer between source and drain regions thereof.

Response to Arguments

7. Applicant's arguments filed on 07/20/04 have been fully considered but they are not persuasive.

In response to applicant's argument that Zhang fails to disclose or suggest that the spacers are formed at a region covered by the black matrix between the first and second substrates, it is respectfully pointed out to applicant that Zhang clearly shows in Fig. 1 that the spacer (112) is formed at a region covered by the black matrix (108) between the first and second substrates. Zhang also discloses (col. 2, lines 21-44) and shows in Fig. 2 that the black matrix overlaps the gate line and the data line and that the

spacer is formed at the intersecting portion of the gate line and the data line. Therefore, it is clear that Zhang discloses and suggests about forming a spacer in a region covered by the black matrix between the first and second substrates. Further, it is also respectfully pointed out to applicant that even though the instant claim does not exactly recite that the spacer is disposed at a region wherein a black matrix overlaps the gate line or the data line, considering the limitations such as, "a black matrix that overlaps the gate line or the data line" and "spacers formed at a region covered by the black matrix between the first insulating substrate and the second insulating substrate", one would easily interpret the limitations as the examiner has interpreted.

Therefore, the rejection was proper and thus maintained.

In response to applicant's request to produce a reference which confirms examiner's assertion that it is common and known in the art to use an organic material with low dielectric constant for forming a passivation layer with flat surface, applicant's attention is respectfully requested to the cited reference USPAT 5,641,974 (col. 5, lines 54-58; col. 6, lines 37-46) which clearly discloses the use of a passivation layer that comprises organic insulating material and has a low dielectric constant.

In response to applicant's argument that the AAPA does not disclose or suggest that a spacer is specifically formed over the black matrix, it is respectfully pointed out to applicant that the AAPA described in the instant application discloses black matrix as well as spacers. Further, even when the spacers are scattered randomly between the substrates, it is desirable that the spacers are arranged at a certain density and for example: a liquid crystal display device having a diagonal size of about 3 inches, the

spacers may be distributed at a density of several tens of pieces per square centimeter which clearly gives a reasonable expectation to one of ordinary skill in the art that the spacers are formed at a region covered by the black matrix and further to maintain a uniform thickness throughout the display it is desirable to place the spacers as dense as possible. Therefore, from the disclosure of the AAPA of the instant application and the knowledge of ordinary skill in the art it would have been obvious that the spacers are formed at a region covered by the black matrix to maintain uniform thickness throughout the display.

Therefore, the rejection was proper and thus maintained.

Applicant's arguments (based on the amendment to the claims) regarding claims 53-56 are persuasive and thus withdrawn.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

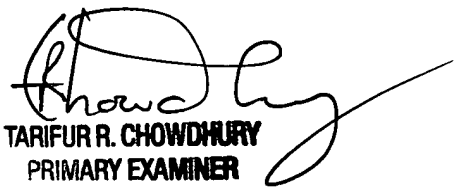
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tarifur R Chowdhury whose telephone number is (571) 272-2287. The examiner can normally be reached on M-Th (6:30-5:00) Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TRC
October 13, 2004



TARIFUR R. CHOWDHURY
PRIMARY EXAMINER